FPGA Based Implementation of Sinusoidal PWM for Induction Motor Drive Applications

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Abstract:
The rapid advances in very large scale integration (VLSI) technology lead to implement modern high speed digital controllers with excellent performance, compared to traditional analog control systems. The field programable gate array (FPGA) devices provide programmable system-on-chip (SoC) environments for designing powerful ASIC controllers with dedicated architectures. This paper presents a FPGA-based digital controller proposed to control induction three-phase motor drives using a single SPARTAN FPGA chip. The sinusoidal pulse width modulation (SPWM) method is realized on FPGA to generate controlling switching pulses for insulated-gate bipolar transistors (IGBTs) in drive system implementing a Verilog hardware description language (HDL) code. The experimental and simulation results demonstrate the efficiency of FPGA-based solutions for implementing dedicated SPWM controller for induction motor drive systems.

Keywords: Field Programmable Gate Array, Sinusoidal PWM, Hardware Description Languages, Verilog, Induction Motors, Drive.

1. Introduction

The induction motors are mainly employed in industrial processes as actuators and final elements due to their desirable performance features. Design and implementation of digital controllers for drive systems is a challenging issue for employing induction motors in industries. The digital signal processors (DSPs) have been mainly utilized by engineers and researchers for controlling induction motors. Nowadays, the field programable gate array (FPGA) chips are quite mature for the industrial electronic and control applications caused by fast progress in very large scale integration (VLSI) technology. Fratta et al. provided a comparative analysis among DSP and FPGA-based control capabilities in PWM power converters. In Simulink-based modeling and simulation of FPGA-based variable-speed drive systems was presented. Chen and Lin implemented the FPGA-based ultrasonic motor servo drive. Real-time FPGA-based high speed motion control was proposed by Yau et al. in. Fung et al. presented FPGA-based adaptive back-stepping fuzzy control for a micro-positioning Scott-Russell mechanism. Bomar implemented a micro-programmed control in FPGAs. Kung and Tsai proposed a FPGA-based speed control IC for PMSM drive with adaptive fuzzy control. FPGA implementation of an embedded robust adaptive controller for autonomous omni-directional mobile platform was presented by Huang and Tsai. Kung et al. realized a motion control IC for X-Y table on FPGA.

Therefore FPGAs are successfully used for implementing induction motor drives due to providing programmable system-on-chip (SoC) environments by incorporating the programmability of programmable logic devices (PLDs) and the architecture of gate arrays. The FPGAs consist of thousands of logic gates and some configurable logic blocks (CLBs) which make them an appropriate solution for prototyping the application-specific integrated circuit (ASIC) controllers with dedicated architectures for specified applications. The circuits and algorithms can be developed in the hardware description languages like VHDL and Verilog which are technology independent.

Monmasson et al. reviewed the FPGA-based design methodologies for industrial control systems. Naouar et al. surveyed FPGA-based current controllers for AC machine drives. They concluded improving the quality of the regulated current in ON-OFF current controllers, proportional-integral (PI) current controller, and predictive current controller due to reduction of the execution time delay from the possibility offered by FPGAs. Although the FPGA-based digital designs have some merits than microprocessor circuits, pointed in literature, including programmability, rapid prototyping, fast time-to-market, embedding processor, low power consumption, low cost and higher density for the implementation of the digital systems. But the concurrent operation,ASIC controller design and simultaneously processing are the main reasons of authors for employing FPGA for implementing induction motor derives.

The rest of the paper is organized as follows. Section presents a synoptic architecture of FPGA-based drive
system for \( \tau \)-phase induction motor followed by a description of sinusoidal PWM. The realization of SPWM on FPGA, the Verilog-based modules and the simulation results achieved by ISE for each module are presented in section \( \tau \). The experimental set up and practical results are described in section \( \tau \). Finally the paper is concluded in section \( \tau \).

\( \tau \). FPGA Based Motor Drive Solution

The main parts of the FPGA-based solution for ac motor drive applications are described in this section. Figure \( \tau \) shows a synoptic of the proposed drive system which consists of FPGA control board and motor driver board. The FPGA control board provides the switching signals for insulated-gate bipolar transistors (IGBTs) of inverter block using sinusoidal PWM. The switching frequency, the dead time of IGBTs and the phase selection are managed by FPGA. The FPGA control board includes an intellectual property (IP) core for managing digital interfaces by ADC modules and other digital measurements. The motor driver board consists of three main modules which are inverter block, power system and analog to digital converters.

\( \tau \). The Insulated Gate Bipolar Transistors (IGBTs)

The power electronic drive includes \( \tau \)-puls \( \tau \)-level IGBTs for voltage-source converter. The IGBTs \([\tau \tau]\) are used in switched mode for drive applications where the forward characteristic of the IGBT can be represented by a linear substitute characteristic \([\tau \tau]\), shown in figure \( \tau \).

\[
V_{CEe}(t) = V_{CE}(T) + R_{CE}I_C(t)
\]

where \(R_{CE}\) is the device on-state resistance and \(V_{CE}(T)\) is the collector-emitter threshold voltage. Another important characteristic of an IGBT for electronic drive is the timing chart for switching operation of the device during turn-on and turn-off, respectively.

\( \tau \). The Sinusoidal Pulse Width Modulation (SPWM)

In SPWM approach a sine wave is employed as reference signal which is compared to a triangular carrier signal to provide High-Low pulses, shown in figure \( \tau \). The output signal, \(V_s\), is high when the amplitude of reference signal, \(A_r\), is greater than that for carrier signal, \(A_c\), otherwise is low.

\[
V_s = \begin{cases} 
\text{High}, & A_r \geq A_c \\
\text{Low}, & A_r < A_c 
\end{cases}
\]

The modulation index is defined as \(M = \frac{A_r}{A_c}\). By changing modulation index from \(\cdot\) to \(\tau\) the output voltage changes from \(\cdot\) to \(V_s\) which could be used for voltage control of motor.

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**Fig. \( \tau \)** The linear characteristic of a typical IGBT in switching mode

**Fig. \( \tau \)** The High-Low pulse generation by SPWM approach.

**Fig. \( \tau \)** Synoptic of the FPGA based drive system
**1. FPGA Realization of SPWM**

This section describes the practical aspects of realization the SPWM based drive approach on FPGA. A Verilog HDL code was implemented into six modules which are instantiated in an IP core.

**1.1 The SINE module**

This module generates a discrete sine wave by providing \( \pi \) samples of a sine wave from \( \alpha \) to \( \pi \) degrees. The frequency of sine wave varies between \( \gamma \cdot \text{HZ} \) to \( \varphi \cdot \text{Hz} \), i.e. \( f \in \left[ \gamma, \varphi \right] \text{Hz} \), and SINE module refreshes itself each \( \frac{1}{f} \) second. Figure 4 shows the behavior of SINE module for providing discrete samples of sine waves.

![Fig. 4 Providing discrete samples of sine waves by SINE module](image)

**1.2 The PWM module**

The outputs of SINE are connected to PWM module to provide pulse width modulation signals. The PWM module consists of an up/down counter which counts from \( \alpha \) to \( \gamma \), then changes its direction and counts until \( \alpha \) in \( \frac{1}{f} \) second, where \( f \) is frequency of the SINE module. The clock pulse of PWM module is \( \delta \gamma \) times faster than \( f \). The up/down counter makes a triangle wave that is used as carrier signal. The voltage of motor and consequently the speed of motor could be adjusted by modulation index (M). Figure 5 shows the pulse width modulation signals provided by PWM module.

![Fig. 5 The pulse width modulation signals provided by PWM module](image)

**1.3 The DEAD-TIME Module**

In power circuit there are \( \gamma \) insulated-gate bipolar transistors (IGBTs) where each phase needs two IGBTs. Practically the IGBTs have dead times called \( t_d \) for switching from high to low which is around \( \mu \text{s} \). This time is considered for preventing of sending both high and low signals to IGBTs in the same time which damages the power circuit. The DEAD-TIME module receives PWM outputs and provides \( \mu \text{s} \) delay time for turning IGBTs, shown in figure 6.

![Fig. 6 The \( \mu \text{s} \) delay time provided by DEALY module](image)

**2. The PHASE-CNTR Module**

This module enables each phase when the previous one is in \( \gamma \) degrees position. Figure 7 shows the phase enabling by the proposed module in appreciate time.

![Fig. 7 Phase enabling by PHASE-CNTR module](image)

**3. The DIRECTION Module**

The outputs of the DEALY module are connected to the DIRECTION module for changing motor rotation direction shown in figure 8.

![Fig. 8 The changing motor rotation direction](image)

**4. The FREQ_DIVIDER module**

This module provides the frequencies that are needed for SINE and PWM modules from oscillator signal. The motor speed could be controlled by changing the output frequency of FREQ_DIVIDER module. This module can adjust motor frequency from \( \gamma \cdot \text{Hz} \) to \( \varphi \cdot \text{Hz} \). Figure 9 shows different clock generation by FREQ_DIVIDER module.

![Fig. 9 The different clock generation by FREQ_DIVIDER module](image)
Experimental Results

This section presents the results of implementation the SPWM approach on FPGA for \( \tau \)-phase induction motors drive. The experimental set up consists of two main parts; the FPGA controlling board for providing switching pulses and the power circuit board. The characteristics of the motor were given in Table 1. The digital control system was implemented on SPARTAN \( \tau \) chip number XC3S004-10Q208, from Xilinx Inc. The Xilinx ISE 1.01 Web-Pack edition was used for synthesized the Verilog programs.

<table>
<thead>
<tr>
<th>KW</th>
<th>HZ</th>
<th>RPM</th>
<th>V</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>73.0</td>
<td>0.082</td>
<td>360</td>
<td>9.1</td>
<td>( \Delta /.1 )</td>
</tr>
</tbody>
</table>

Figure 11(a) shows the internal architecture of the proposed FPGA implementation of motor drive IC. The internal circuit block diagram comprises the main modules to perform the function of the SPWM for drive the IGBTs, generate the frequency, collect the response data, and communicate with external devices.

Figures 11(a) and 11(b) show the switching signals that were exerted to each phase IGBTs and the signals which were exerted to a low pass filter with \( C=0.01 \) nf and \( R=1 \) K\( \Omega \), respectively. As shown in figure 11(a) the switching pulses of one leg IGBTs in the inverter circuit are not high and low in the same time. Furthermore, the frequency and the amplitude of these pulses could be adjusted by FPGA for controlling the speed of motor.
δ. Conclusion
In this paper, the successful digital design and implementation of a programmable Sinusoidal PWM control IC for induction motor drives have been demonstrated. The FPGA technology has been employed for implementing the Sinusoidal PWM control IC using hardware description language Verilog approach. The simulation and experimental results verified the effectiveness of implemented ASIC SPWM control IC with dedicated architecture. The proposed SPWM IC can generate a wide range of PWM output voltages and frequencies which could be applied for motor speed control. The proposed FPGA-based digital control scheme is flexible, low cost, and high performance for induction motor drive applications.

References