Designing CMOS folded-cascade operational amplifier
And Implementation with CMOS
Technology in IC

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Abstract: In this paper a new high gain bandwidth (GBW) and low power folded cascade OPAMP is presented. It has been implemented and layed out by CADENCE software in 0.18µm. Its DC gain is 82db and its bandwidth is 200MHz. Power consumption is one of the main design challenges in very-low-voltage high-speed analog integrated circuits. In this paper, different techniques to reduce the power consumption in low-voltage fast settling operational amplifiers for switched-capacitor applications are discussed. These techniques include a novel dynamic allocation of settling time parameters. Design considerations for a 1.5-V low-power operational amplifier merging these techniques are addressed. Simulation results of the circuit in a 0.025-mm CMOS process confirm the effectiveness of the approaches to considerably reduce the power consumption of high-speed operational amplifiers. Finally, the op-amp has been used in an integrator of a first order sigma-delta modulator analog to digital convertor (ADC) and has been tested. Its result confirms our idea and modified OP-AMP improve 10 DB output SNR of sigma-delta modulator rather than older OP-AMP.

Keywords: OPAMP, gain bandwidth, low voltage, switch capacitor, settling time.

I. Introduction

Power consumption is one of the most challenging issues in modern portable electronic equipment. Reduction of the power dissipation looks even more challenging in low-voltage analog integrated circuits, as there will be less room for the signal and to keep the same signal-to-noise ratio, the power is to be increased. The power consumption is also increased when the operating speed is increased. Therefore, low-power design approaches for low-voltage fast-settling operational amplifiers in switched-capacitor applications can be very attractive. In this paper, low-power design techniques for a low-voltage fast-settling operational amplifier are discussed and a 1.5-V low-power very fast-settling operational amplifier for the first stage of a high-resolution sigma-delta A/D converter is presented.[1] Operational amplifier (Op-Amp) is one of the basic and important circuits which has a wide application in several analog circuits such as switched-capacitor filters, algorithmic, pipelined and sigma-delta A/D converters, sample-and hold amplifiers, and etc. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the Op-Amp; the larger bandwidth and gain, the higher speed and accuracy.[1] Depending on the required specifications, several Op-Amp structures have been designed; one of mostly used circuit named folded cascode is illustrated in Fig. 1. Some advantages of this structure are: large –3 dB frequency and unity gain bandwidth (UGBW), high input common-mode range, and high output swing. In order to operate at high frequencies, it is necessary to use the transistors with minimum channel length [2], [3], which results in a DC gain of 40–50 dB in a typical 0.35 µm technology (depending on the overdrive voltage of the devices); this is not enough in most applications [3]–[4]. The gain boosting method known as super cascode [2], uses a special technique to increase the output resistance and therefore the DC gain; But this method causes the –3 dB frequency to become lower by the same ratio of gain boosting and has no improvement on the UGBW. As another alternative, by increasing the channel length of transistors and therefore reducing the channel length modulation, the output resistance and consequently the gain are increased; but this causes the internal capacitances of transistors to become larger and the frequency response is degraded [3], [4].

The paper is organized as follows: in Section.2, a brief
analysis of the conventional folded cascode is given; Section 3 presents the basic idea in the new Op-Amp circuit along with the corresponding analytical equations; simulation results and layout of this IC and test of OP-AMP in first order sigma-delta modulator are given in Section 4, and finally Section 5 conclude the paper.

II. Conventional Folded Cascode

Because of high performance and wide applications, the detailed analysis of this structure is performed in several references [1], [2], [4]. By applying good approximations, the voltage gain of the Op-Amp is given by:

\[ A_v \approx g_{m1}R_o \]  
\[ R_o \approx \left[ g_{m7}r_{o7}\left(r_{o1} - r_{o9}\right)\right] \left( g_{m5}r_{o5}r_{o3}\right) \]  
\[ g_{m1} = \sqrt{2\beta I_1} \]

That \( \beta = \mu C_{ox}\left(\frac{W}{L}\right) \), \( \mu \) is the mobility of electrons, \( C_{ox} \) is thin oxide gate capacitor and \( W/L \) is aspect ratio of transistor. In this analysis the channel length modulation effect will be neglected. Because our channel’s transistors are not short (\( L \geq 1 \mu m \)) and channel-length modulation is inversely proportional to the channel length transistors. These large lengths also reduce the mobility degradation effects and conductance of transistors. Despite this, the influence of these effects in the circuit will become apparent in the simulation results of the circuit.

Studying of the frequency response:[2]:

1. First pole: Because of high output resistance of the circuit \( R_o \), first pole occurs in this node:
   \[ \omega_1 = \frac{1}{(R_oC_o)} \]  

2. Second pole: Happens in the cascode node (drain of \( m_1 \)), with a frequency of much greater than the first pole. Therefore output capacitance bypasses the effect of output resistance, and causes to appear an equivalent resistance of approximately \( 1/g_{m7} \) from the source of \( m_7 \). Hence:
   \[ \omega_2 = -1/(R_{cascode}C_{cascode}) \]  
   \[ C_{cascode} = C_{d1} + C_{d7} + C_{s7} \]  
   \[ R_{cascode} \approx \left( 1/g_{m7}\right) \left( r_{o1} - r_{o9}\right) \left( r_{o3}\right) \]

3. Zero: Because of existing a second signal path through \( C_{gd1} \), a right half plane zero is introduced to transfer function whose frequency is calculated as:
   \[ \omega_z = g_{m1}/C_{gd1} \]

Note that the pole related to input terminals due to series resistance of signal source, and the pole and zero caused by PMOS cascode loads (current sources “\( m_3 – m_5 \)” & “\( m_4 – m_6 \)”), have no considerable effect on the frequency response and are ignored. In a typical 0.35 \( \mu m \) CMOS process, a voltage gain of 100–300, and UGBW of approximately 700MHz with a phase margin of 75° for a capacitive load of 1 pF is achievable (the bias current of the branches is \( I = 1mA \))[1].

III. Modified OP-AMP

In this paper for low power design and high gain approach transistors \( \left(\frac{W}{L}\right) \) exactly. If transistors \( \left(\frac{W}{L}\right) \) be high, frequency bandwidth will be decreased and if transistors \( \left(\frac{W}{L}\right) \) be low, gain will be decreased and power will be increased. It’s a trade off between bandwidth and gain-power.

Figure 2: modified op-amp
\[ V_{out+} = R_{out} \times G_m \times V_{diff} \quad (10) \]

That \( G_m \) introduced by (3) and \( R_{out} \), \( V_d \) introduced by:

\[ R_{out} \cong r_{o7} \times r_{o4} \times g_{m7} \left| r_{o5} \times r_{o3} \times g_{m3} \right| \quad (11) \]

\[ V_{diff} = \frac{V_{in+} - V_{in-n}}{2} \quad (12) \]

**A. DC characters and transient response**

In this case, we try to design a low power and low voltage op-amp. Minimum op-amp’s VDD must be:

\[ VDD_{min} = V_{OD3} + V_{OD5} + V_{OD7} + V_{OD9} \quad (13) \]

\[ V_{OD3} = \frac{2I_f}{\beta} \quad (14) \]

This op-amp tested by a sinus voltage 10\( \mu \) volt amplitude and 50k hertz frequency and 0.8 volt offset. Its result is shown in figure 3. For frequency test we put designed op-amp in a unique feedback and we see the circuit is stable and negative input followed positive input with very low error. (figure 4)

**B. Common Mode Feedback (CMFB)**

In every op-amp for adjust output offset and hold output stage transistors in saturation region we have to use a Common Mode Feedback (CMFB). In many op-amp circuits for getting trust feedback, we need equal input and output offset. A CMFB get feedback \( V_{out+}, V_{out-} \) from output stage and by adjusting \( V_{gs} \) of M11 and M12, fixed dc output \( V_{out+}, V_{out-} \) in our favourite voltage. Figure 5 shows CMFB used in this work. In switch capacitor CMFB, in first phase, \( V_{out+}, V_{out-} \) measured by \( C_1 \) and in second phase, \( V_{gs} \) of M11 and M12 adjusted by \( C_2 \).

![Figure 3: output (left) and input (right) of test circuit op-amp](image1)

![Figure 4: output+ and output- in unit negative feedback of op-amp](image2)
Frequency Response

In this paper, because of distance first and second pole of circuit, the op-amp doesn’t need to frequency compensation. Frequency compensation with capacitor and resistor caused some problem such as decreasing bandwidth and creating right-hand pole. So, in this paper we don’t have this problem.

In figure 6 we show Frequency Response and circuit phase margin.

C. Circuit Layout

In this paper we layouted circuit op-amp with CADENCE software in TSMC 0.18µm technology and checked transient and frequency response of real circuit layouted and schematic circuit. And the result with good approximate is same (fig.7).

Finally for operational test, we put designed op-amp in integrator circuit of a sigma delta modulator. We considered designed op-amp has worked correctly. Fig.8 shows block diagram of sigma-delta modulator analog to digital convertor (ADC). In figure 9 input and output of a first order one bit quantizer sigma-delta modulator is showed.

IV. SIMULATION RESULT

A. First Order Sigma-Delta with Modified Op-Amp

First order sigma-delta modulator consist a loop filter and one bit quantizer and a DAC (fig.8). Output of modulator can be calculated by:

\[ Y(Z) = STF(Z)X(Z) + NTF(Z)E(Z) \]  \hspace{2cm} (15)

For testing designed op-amp, it has been put in first order sigma-delta modulator, and the circuit has been tested for a sinuous signal with \( f_{in} = 1 \text{ kHz} \) and sampling frequency \( f_s = 500 \text{ kHz} \) (fig.9). In fig.10, transient response of the modulator has been shown. By calculating PSD of transient response of modulator output by fast Fourier transform (FFT) (fig.11) signal to noise ratio (SNR) and effective number of bits (ENOB) has been calculated:

\[ SNR = 10 \log \left( \frac{|P_{signal}|}{|P_{noise}|} \right) = 10 \log \left( \frac{|P_{signal}|}{P_{total} - P_{signal}} \right) \]  \hspace{2cm} (18)

\[ SNR = 53.812 \text{ DB} \]  \hspace{2cm} (19)

\[ ENOB = 8.637 \text{ bit} \]  \hspace{2cm} (20)

\[ STF(Z) = \frac{Y(Z)}{X(Z)} = \frac{1}{1 + \frac{1}{Z^{-1}}} = Z^{-1} \]  \hspace{2cm} (16)

\[ NTF(Z) = \frac{Y(Z)}{E(Z)} = \frac{1}{1 + \frac{1}{Z^{-1}}} = 1 - Z^{-1} \]  \hspace{2cm} (17)
V. CONCLUSION

In this paper a new low power high gain bandwidth op-amp is designed and layouted in CADENCE with 0.18µm technology. Finally, this op-amp has been put in first order sigma-delta modulator as integrator and transient output and PSD of its output has been simulated. its SNR and ENOB has been calculated. In equation (21), (22) SNR and ENOB of first order modulator fig.9 by considering Conventional op-amp in ref [2] as its integrator of loop filter has been calculated:

\[
\text{SNR}_{\text{Conventional op-amp in ref[2]}} = 43.345 \text{ DB} \quad (21)
\]

\[
\text{ENOB}_{\text{Conventional op-amp in ref[2]}} = 6.90 \text{ bit} \quad (22)
\]

it proofs that designed op-amp has improved 10DB in SNR rather than older op-amp in fig1.

VI. References

[1]. Reza Lotfi*, Mohammad Taherzadeh-Sani, M. Yaser Azizi, Omid Shoaei, "Low-power design techniques for low-voltage fast-settling operational amplifiers in switched-capacitor applications", INTEGRATION, the VLSI journal 36 (2003) 175–189